STELLA MARIS COLLEGE (AUTONOMOUS), CHENNAI – 600 086
(For Candidates admitted during the academic year 2008-09)

SUBJECT CODE : CS/MC/CO34

B.C.A. DEGREE EXAMINATION – NOVEMBER 2009
THIRD SEMESTER

REG. NO.: _____

COURSE : MAJOR CORE
PAPER : COMPUTER ORGANIZATION
TIME : 20 MINUTES **MAX. MARKS: 20**

SECTION – A
ANSWER ON THE QUESTION PAPER ITSELF:

ANSWER ALL THE QUESTIONS: **20X1=20**

Choose the best answer:

1. Time needed to execute a program is called as _____ time
   a) Processor b) CPU c) Control d) Access

2. Address of the next instruction to be executed is given by _____
   a) Address Register b) Accumulator c) Program Counter d) Register

3. The range of memory locations that can be accessed using n bits is _____
   a) $0-2^{n+1}$ b) $0-2^{n}+1$` c) $0-2^{n-1}$ d) $0-2^{n}-1$

4. Storage mechanism of queue is _____
   a) FCFS b) LIFO c) FIFO d) Both a and c

5. When a location other than a destination operand in an instruction is affected the instruction is said to have a _____
   a) Data Hazard b) Auto increment addressing
   c) Data Dependency d) Side effect

6. Repeatedly executed instructions in a particular area of a program is called as _____
   a) Cache Block b) Locality of Reference c) Cache Line d) Cache Area

7. Determining the color and intensity of each image pixel is known as ____
   a) Rendering b) Projection c) Sampling d) Clipping

8. The mechanism of representing one bit by an electrical signal that has one of two voltage values is called as _____
   a) Broadband b) Baseband c) Modulation d) Demodulation

9. I/O interrupts are one example of a _____
   a) Exception b) Interruption c) Signals d) Privileged Instructions

10. The arrangement of memory and I/O devices sharing the same address space is referred as _____
    a) Interface b) I/O mapped I/O
    c) memory – mapped I/O d) Program-controlled I/O

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Fill in the blanks:

11. The term cycles per second is called _____.
12. Using lower byte addresses for the less significant bytes is known as _____.
13. A technique called _____ can minimize the penalty incurred as a result of conditional branch instruction.
14. The _____ rate refers to the number of symbols transmitted per second.
15. The Processor, Memory and I/O devices are interconnected by means of a _____.

State True or False:

16. Reducing the amount of processing done is one basic step which increases the clock rate.
17. Zero flag is set to zero if the result is zero.
18. Cache block is also known as cache line.
19. The smallest addresseable spot in the screen is called a texels.
20. A Process is a program in execution.

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TIME : 2 HOURS & 40 MINUTES **MAX. MARKS: 80**

SECTION – B

ANSWER ANY EIGHT QUESTIONS: **8X5=40**

1. List out the functions of system software.
2. Write short notes on Basic Performance Equation
3. With examples explain the basic instruction types
4. Discuss about how a source program is assembled into an object program
5. Give the steps of processing each instruction by a pipeline processor
6. Write short notes on ROM and its types
7. Explain any two input and output devices
8. Give the various schemes in which a communication link may be operated
9. Explain Polling and Vectored Interrupts
10. Explain the handshake control of data transfer during an input operation

SECTION – C

ANSWER ANY FOUR QUESTIONS: **4X10=40**

11. With a neat diagram explain the functional unit of a computer system
12. Explain the different types of addressing modes with examples
13. Briefly discuss about the Pipeline Performance. Also explain data hazards with a neat diagram
14. Explain Address Translation in Virtual memory with a neat diagram
15. Write short notes on synchronous and Asynchronous transmission
16. Explain DMA

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