

B.C.A. DEGREE EXAMINATION – NOVEMBER 2010
THIRD SEMESTER

REG. NO.: _____

COURSE : MAJOR CORE
PAPER : COMPUTER ORGANIZATION
TIME : 20 MINUTES

MAX. MARKS: 20

SECTION – A
ANSWER ON THE QUESTION PAPER ITSELF:

ANSWER ALL THE QUESTIONS: 20X1=20

I Choose the correct answer

- Actual execution of instructions in a computer takes place in _____
a) ALU b) Control unit c) Memory unit d) I/O unit
- The processor in which large number of complex instructions are available is
a) RISC b) CISC c) Hardwired d) Microprogrammed
- The operation involving the memory that transfers a copy of the contents of a specific memory location to the processor is
a) Store b) Move c) Load d) Copy
- The processor contains a register called the _____, which holds the address of the instruction to be executed next.
a) Instruction register b) program counter c) buffer d) None of the above
- The fastest small memory is
a) Main b) Associative c) Cache d) Virtual
- The instruction ADD X represents
a) Stack organization c) General register organization
b) Single accumulator organization d) None of the above
- Which one of the following input devices is used to capture images and store them as digital data?
a) Scanners b) Trackball c) Joystick d) mouse
- A communication link that allows transmission in either direction, but not at the same time is
a) Full duplex b) Half Duplex c) Simplex d) None of the above
- Name the bus arbitration in which all units are connected to a single BUS REQUEST
a) Polling b) Daisy chaining c) Independent questing d) none of the above
- In _____ the interface transfers data into and out of the memory unit through the memory bus
a) Interuupt-initiated I/O b) Programmed I/O c) DMA d) I/O processor

II Fill in the blanks

11. A group of lines that serves as a connecting path for several devices is called a _____
12. A _____ is a list of data elements, with the accessing restriction that elements can be added or removed at one end of the list only.
13. The performance of a cache memory is frequently measured in terms of a quantity called _____.
14. VGA stands for _____.
15. When I/O devices and the memory share the same address space, the arrangement is called _____.

III State True or False

16. Processor circuits are controlled by a timing signal called a clock.
17. Machine language use symbolic names and mnemonics.
18. Auxiliary memory is the central storage unit in a computer system.
19. OpenGL is an example of API standards.
20. Each I/O device connected to the computer is assigned unique set of address.

STELLA MARIS COLLEGE (AUTONOMOUS), CHENNAI – 600 086
(For Candidates admitted during the academic year 2008-09 & thereafter)

SUBJECT CODE: CS/MC/CO34

B.C.A. DEGREE EXAMINATION – NOVEMBER 2010
THIRD SEMESTER

COURSE : MAJOR CORE
PAPER : COMPUTER ORGANIZATION
TIME : 2 HOURS & 40 MINUTES **MAX. MARKS: 80**

SECTION – B

ANSWER ANY EIGHT QUESTIONS: 8X5=40

1. What is a bus? Explain single bus structure.
2. Explain how the performance of computers is measured using Benchmark programs.
3. Explain how instructions are sequenced and executed?
4. Explain how condition code flags are used by the processor to keep track about the results of branch operations.
5. Discuss the implementation of memory stack.
6. Explain with an example arithmetic pipeline.
7. Explain the principle and working of non-impact printers.
8. Write a short account of joystick and touchpad.
9. Illustrate the concept of Interrupts with an example.
10. Discuss briefly Synchronous bus.

SECTION – C

ANSWER ANY FOUR QUESTIONS: 4X10=40

11. Explain the different functional units of a digital computer.
12. Define addressing mode. Explain the various addressing modes with examples.
13. Discuss the various mapping techniques used in the organization of cache memories.
14. Explain Associative memory and illustrate how reading and writing takes place.
15. Explain Synchronous and asynchronous data transmission.
16. Explain DMA and the use of DMA controllers in a computer system.
