STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2015-16)

SUBJECT CODE : 15PH/MC/EL14

B.Sc. DEGREE EXAMINATION NOVEMBER 2015
BRANCH III - PHYSICS
FIRST SEMESTER

REG. No._____

COURSE : MAJOR – CORE
PAPER : ELECTRONICS – I
TIME : 30 MINS. MAX. MARKS : 30

SECTION – A
TO BE ANSWERED IN THE QUESTION PAPER ITSELF

ANSWER ALL QUESTIONS: (30 x 1 = 30)

I CHOOSE THE CORRECT ANSWERS:

1. In the 8-4-2-1 BCD code, the decimal number 125 is written as
   (a) 1111101 (b) 000100100101 (c) 7D (d) none of these

2. 0111 is an excess -3 of
   (a) 7 (b) 10 (c) 3 (d) 2

3. In a half adder having two inputs A and B and two outputs (S and C are the sum and carry output bits respectively), the Boolean expression for S and C in terms of A and B is
   (a) $S = \bar{A}\,B + A\bar{B},\ C = AB$ (b) $S = AB + \bar{A}\bar{B},\ C = A + B$
   (c) $S = \overline{AB} + AB,\ C = A + \bar{B}$ (d) $S = \bar{A} + \overline{AB},\ C = \bar{A} + \bar{B}$

4. The dual of the Boolean theorem $A \cdot (B + C) = AB + AC$ is
   (a) $A \cdot (B + C) = AB + AC$ (b) $A \cdot (B + C) = (A + B)(A + C)$
   (c) $A \cdot BC = (A + B)(A + C)$ (d) none of these

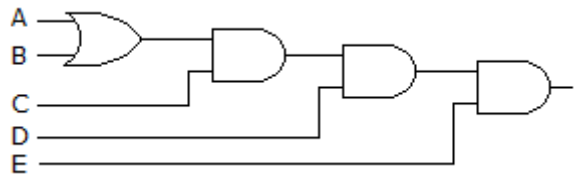
5. A full-adder can be implemented with half-adders and OR gates. A 4-bit parallel full-adder without any initial carry requires
   (a) 8 half-adders and 4 OR gates (b) 8 half-adders and 3 OR gates
   (c) 7 half-adders and 4 OR gates (d) 7 half-adders and 4 OR gates

6. A 4-bit Mod -16 ripple counter uses a J-K flip-flop. If the propagation delay of each flip-Flop is 50 ms, the maximum clock frequency is equal to
   (a) 20 MHz (b) 10 MHz (c) 5 MHz (d) 4 MHz

7. A ring counter is same as
   (a) up-down counter (b) parallel counter (c) shift registers (d) none of these

8. How many flip-flops are required for dividing the frequency by 64?
   (a) 4 (b) 5 (c) 6 (d) 8

9. Derive the Boolean expression for the logic circuit shown below:



(a) $C(A + B)DE$ (b) $[C(A + B)D + \bar{E}]$ (c) [C(A+B)D]$\bar{E}$ (d) ABCDE

..2

10. One of De Morgan's theorems states that. $\overline{X+Y} = \bar{X} \cdot \bar{Y}$ Simply stated, this means that

logically there is no difference between:
(a) a NOR and an AND gate with inverted inputs
(b) a NAND and an OR gate with inverted inputs
(c) an AND and a NOR gate with inverted inputs
(d) a NOR and a NAND gate with inverted inputs

11. How is the number one (1) indicated on the outputs of a 7447 BCD-to-seven-segment code converter?
(a) Segment a is active (b) Segment b is active.
(c) Segments a and b are active (d) Segments b and c are active

12. Which is not a MOSFET terminal?
(a) Gate (b) Drain (c) Source (d) Base

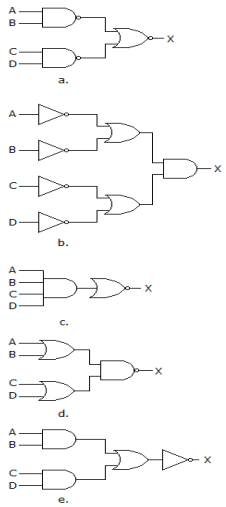
13. PMOS and NMOS circuits are used largely in
(a) MSI function (b) LSI function (c) diode function (d) TTL function

14. Add the following BCD numbers.

0110	0111	1001
0101	1000	1000

(a) 0000 1011 0000 1111 0001 0001
(b) 0001 0001 0001 0101 0001 0001
(c) 0000 1011 0000 1111 0001 0111
(d) 0001 0001 0001 0101 0001 0111

15. Which of the figures in figure (a to d) is equivalent to figure (e)?



(a) a (b) b (c) c (d) d

II FILL IN THE BLANKS:

16. A circuit that can convert one of ten numerical keys pressed on a keyboard to BCD is a _____.
17. The Boolean expression $A\bar{B}(A+\bar{B})$ can be reduced to _____.
18. Assume a LOW logic level is placed on the SHIFT/LOAD input of a 74195 shift register. The output will change_____.
19. When the output of the NOR gate S-R flip-flop is in the HOLD state (no change), the inputs are _____.
20. Assume that you have a 3-input NAND gate but need only a 2-input gate. The unused input should be _____.

III STATE WHETHER TRUE OR FALSE:

21. In true sum-of-products expressions, the inversion signs cannot cover more than single variables in a term
22. The product-of-sums (POS) is basically the OR ing of AND ed terms
23. A universal shift register has both serial and parallel input and output capacity
24. The J-K flip-flop is a standard building block of clocked (sequential) logic circuits known as logic standard primitives
25. CMOS is a more dominant IC technology than TTL

IV ANSWER BRIEFLY:

26. Which gates are called as the universal gates? What are its advantages?

27. What are basic properties of Boolean algebra?

28. What are called don't care conditions?

29. What is Demultiplexer?

30. Define state diagram.

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TIME : 2 ½ HOURS **MAX. MARKS : 70**

SECTION – B

ANSWER ANY FIVE QUESTIONS: **(5 x 5 = 25)**

1. Represent the following Boolean expression by K-map
   $Y(A,B,C,D) = (A + B + \bar{C})(\bar{A} + C + \bar{D})$
2. Represent the following decimal numbers in 1's complement representation using eight bits.
   (a) -67 (b) 102
3. Draw and explain the 4-bit parallel adder using IC74182.
4. Draw the logic circuit of S-R flip-flop using D flip-flop.
5. A uniformly doped n-type silicon epitaxial layer of 0.5 ohm-cm resistivity is subjected to a boron diffusion with constant surface concentration of 5 x 10^{18} cm^{-3}. It is desired to form a p-n junction at a depth of 2.7 x 10^{-6} m. At what temperature should this diffusion be carried out if it is to be completed in 2 hour?
6. Draw a clocked J-K flip-flop system and include preset (Pr) and clear (Cr) inputs and explain the clear operation
7. Prove the following Boolean theorems
   (a) $(A + B)(A + \bar{B})$ (b) $AB + \bar{A}C = (A + C)(\bar{A} + B)$ (c) A(A+B) = A

SECTION – C

ANSWER ANY THREE QUESTIONS: **(3 x 15 = 45)**

8. Explain the rules of 2's complement addition and subtraction with suitable example.

9. Draw and explain the carry look-ahead adder.

10. Write down the simplified Boolean expression in (a) SOP form and (b) POS form for :
    (i) $Y(A,B,C,D) = \sum m\,(1,4,6,9,10,11,14,15)$
    (ii) $Y(A,B,C,D) = \prod M\,(0,1,3,5,7,9,10,11,12,13,15)$

11. Explain how a J-K flip-flop is converted into D flip-flop and T flip-flop.

12. Draw the logical diagram of 4 bit shift register. Explain how shift-left and shift-right operations are performed.

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