STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2004-05 & thereafter)

SUBJECT CODE : **PH/MC/MI54**

B.Sc. DEGREE EXAMINATION NOVEMBER 2008
BRANCH III - PHYSICS
FIFTH SEMESTER

REG. No._____

COURSE : **MAJOR – CORE**
PAPER : **MICROPROCESSORS**
TIME : **30 MINS.** MAX. MARKS : **30**

SECTION – A

TO BE ANSWERED IN THE QUESTION PAPER ITSELF

ANSWER ALL QUESTIONS: (30 x 1 = 30)

I CHOOSE THE CORRECT ANSWER:

1. 8 BIT Microprocessor 8085 has, X number of lines in the ADDRESS bus & Y number of lines in the DATA bus
   a) X=8 & Y=8 b) X=8 & Y=16 c) X=16 & Y=16 d) X=16 & Y=8

2. The role of the Program Counter in 8085 is to
   a) hold the address of top of Stack
   b) point to the vector address
   c) hold the address of the instruction to be fetched next
   d) hold the return address

3. During the operation of a PUSH B instruction.
   a) The content of BC reg pair is increased by ONE
   b) The content of SP reg pair is decreased by ONE
   c) The content of SP reg pair is decreased by TWO
   d) The content of SP reg pair is increased by TWO

4. During MEMORY READ operation is is 8085, the following thing happens:-
   a) IO/M line goes LOW & RD line goes HIGH
   b) IO/M line goes LOW & RD line goes LOW
   c) IO/M line goes HIGH & RD line goes LOW
   d) IO/M line goes HIGH & RD line goes HIGH

5. The execution of the Instruction MVI A, 00 H in 8085 affects
   a) Z flag b) CY flag
   c) S flag d) NONE of the FLAGS

6. The BC reg.pair contains FFEF H. After the execution of the instruction INXB, the content of the registers will be
   a) B = 00 b) C = FF c) C = F0 d) B = EF

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7. The content of Reg.pairHL=8050 H, reg.A=09 H & memory location 8050 H = FF H. After the execution of the instruction INRM, the content of the register / Memory will be
   a) HL = 8051 H
   b) A = 10 H
   c) content of memory 8050 H = 00 H
   d) A = 0A H

8. Executing the Instruction RLC consecutively 3 times, the content of A register gets
   a) multiplied by 3 times
   b) multiplied by 6 times
   c) multiplied by 8 times
   d) divided by 3 times

9. For Partial decoding, number of ADDRESS LINES needed for One 2Kx8 ROM is
   a) 8 b) 10 c) 11 d) 16

10. Maximum number of INPUT ports that can be decoded in direct I/O scheme will be
    a) 256 b) 512 c) 1024 d) 64 K

11. The number of Soft Ware INTERRUPTS available in 8085 is
    a) 4 b) 5 c) 8 d) 16

12. The VECTOR ADDRESS of TRAP interrupt is
    a) 0000 H b) 8000 H c) 0024 H d) 0064 H

13. To have BSR mode of operation with 8255 PPI chip, the Control word is formed with
    a) D_7 Bit=0 b) D_7 Bit = 1 c) D_0 Bit = 0 d) D_0 Bit = 1

14. The Instruction associated with serial out put I/O operation through SOD terminal is
    a) SIM b) RI M c) OUT d) IN

15. Selected Hardware Interrupts can be masked using the following instruction.
    a) SIM b) RIM c) EI d) DI

II FILL IN THE BLANKS:

16. In 8085 the Flag that is not accessible to the user is _____.

17. The Non-Maskable Interrupt in 8085 is called _____.

18. The Instruction that does not have an Execute cycle is _____.

19. The Vector address of the Restart instruction RST1 is _____.

20. The Address is latched during the _____ edge of the ALE control signal.

III STATE TRUE OR FALSE:

21. XCHG instruction exchanges the contents of reg.pairs BC with HL.

22. STACK grows downwards.

23. Memory Fold Back occurs during Partial decoding of I/O devices.

24. In 8255, the BSR mode instruction will affect only PORT C.

25. Instruction DI disables TRAP also.

IV ANSWER THE FOLLOWING BRIEFLY:

26. Write a short note on LIFO Array.

27. Restart Instructions are efficient Call instructions – How?

28. What is a Tri State Buffer?

29. Explain the use of SID and SOD terminals in 8085.

30. How the hardware interrupts in 8085 can be expanded?

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SECTION – B

ANSWER ANY FIVE QUESTIONS: (5 x 5 = 25)

1. Explain the sequence of steps that take place during an Opcode FETCH operation.

2. Explain with suitable examples the Addressing Modes supported by 8085.

3. Explain the micro steps that are executed in various registers inside 8085, while performing a branch instruction CALL, address.

4. Explain the decoder arrangement required to interface Two 8K x 8 Memory device (ROM & RAM) with 8085.

5. Write an Assembly language program to Multiply the content of B reg. By 7_{10} without using ADD instruction.

6. Explain Status Check Mode. Describe the hardware necessary to interface an ADC with 8085 and explain the required Software.

7. Draw the timing diagram for an Instruction MOV A,M and explain the number of T states required for fetching and executing the instruction.

SECTION – C

ANSWER ANY THREE QUESTIONS: (3 x 15 = 45)

8. Bring out the similarities and the differences between the following pairs of instructions:
   a) LDA, address & LHLD, address
   b) LXID, dB & LDAXD
   c) ADD D & DAD D.

9. Write an ALP to Sort an array of positive single bytes stored in memory in Descending order.

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10. Bring out the differences between Direct I/O & Memory mapped I/O. Can an INPUT Port & an OUTPUT Port have the same address? If yes, How? Draw the decoder network.

11. Draw the functional block diagram and explain the salient features available in 8255 PPI chip. Explain the mode 0 operation of 8255 with a suitable application.

12. Explain the different Hardware Interrupts available in 8085. Explain how a Hardware interrupt is acknowledged and executed. Also explain the use of Masking circuits available.

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