

B.Sc. DEGREE EXAMINATION NOVEMBER 2008
BRANCH III - PHYSICS
FIFTH SEMESTER

REG. No. _____

COURSE : MAJOR – CORE
PAPER : ELECTRONICS
TIME : 30 MINS.

MAX. MARKS : 30

SECTION – A

TO BE ANSWERED IN THE QUESTION PAPER ITSELF

ANSWER ALL QUESTIONS:

(30 x 1 = 30)

I CHOOSE THE CORRECT ANSWER:

- In a common base connection $I_E=1\text{mA}$ and $I_C=0.95\text{mA}$. The value of I_B is
a) 1.95 b) 0.95 c) 0.05 d) 0.90
- In a common base connection $I_C=0.95\text{mA}$ and $I_E = 1\text{mA}$. The value of α is
a) 0.05 b) 1.0 c) 1.95 d) 0.95
- The Collector of a NPN Transistor is
a) intrinsic b) lightly doped
c) heavily doped d) moderately doped
- We have β as given by
a) $1/1-\alpha$ b) $\alpha /1-\alpha$ c) $1/1+\alpha$ d) $\alpha /1+\alpha$
- If $\alpha =0.98$, the value of β is as given below
a) 98 b) 50 c) 49 d) 0.02
- If the value of $\beta =50$; and $I_B = 20 \mu$, the value of I_E is given by
a) 1mA b) 1.2mA c) 1.02mA d) 0.98mA
- The point of intersection of a dc and ac load lines is called as
a) Pinch-off point b) Cut-off point c) Operating point d) Firing point
- In a RC coupled voltage amplifier, the voltage gain over mid frequency range is
a) increasing b) decreasing c) constant d) erratic
- Stabilization makes the Operating point,
a) independent b) dependent c) constant d) compensated

10. For Voltage amplification, a Transistor in CE mode should have its collector junction
 - a) forward biased
 - b) reverse biased
 - c) open circuited
 - d) shorted
11. Thermal runaway is caused mainly by
 - a) base current
 - b) collector current
 - c) collector leakage current
 - d) I_E
12. Negative resistance behavior is experienced in the I-V characteristic of
 - a) JFET
 - b) MOSFET
 - c) BJT
 - d) UJT
13. In general a MOSFET can function in the following mode of operation,
 - a) depletion only
 - b) enhancement only
 - c) both depletion & enhanced modes
 - d) none
14. No. of Flip flops required to store a decimal number 2008 in a binary register is
 - a) 4
 - b) 8
 - c) 10
 - d) 11
15. CMRR serves as a figure of merit of a
 - a) voltage amplifier
 - b) power amplifier
 - c) difference amplifier
 - d) current amplifier

II FILL IN THE BLANKS:

16. In a RC coupled amplifier the Capacitor connected in _____ to the emitter Resistance in the self bias arrangement is called the by-pass capacitor.
17. UJT fires when its emitter junction is _____ biased.
18. The Gate-Source junction of a JFET is always _____ biased.
19. The sum of Products form leads to _____ network.
20. In closed loop application of OPAMP, the voltage at its two input terminals are _____.

III STATE TRUE OR FALSE:

21. JFET is a bi-polar device.
22. DC load line is steeper the AC load line.
23. Thermal runaway in encountered in FET also.
24. NOR gate is one of the basic gates.
25. Integrators are preferred over Differentiators is solving differential equations.

IV ANSWER THE FOLLOWING BRIEFLY:

26. Draw the circuit to get an OR function using NAND gate.

27. What happens to the content of a register after performing Left Shift operation Thrice?

28. Why is base of a transistor made thin?

29. Draw the circuit of a unity gain non-inverting amplifier using OP AMP.

30. Define Intrinsic stand-off ratio of a UJT.

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STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2004-05 & thereafter)

SUBJECT CODE : PH/MC/ES54

B.Sc. DEGREE EXAMINATION NOVEMBER 2008
BRANCH III - PHYSICS
FIFTH SEMESTER

COURSE : MAJOR – CORE
PAPER : ELECTRONICS
TIME : 2 ½ HOURS

MAX. MARKS : 70

SECTION – B

ANSWER ANY FIVE QUESTIONS: (5 x 5 = 25)

1. A Transistor is connected in common emitter (CE) configuration in which collector supply is 9V and the voltage drop across resistance R_C connected in the collector circuit is 0.98V. The value of $R_C = 1K\Omega$. If $\alpha = 0.98$ determine:
i) the collector-emitter voltage (V_{CE}) (ii) the base current (I_B).
2. Calculate the emitter current in the voltage divider circuit with the following values. $R_1=10K\Omega$ $R_2=10K\Omega$ $R_C=1K\Omega$ $R_E=5K\Omega$ $V_{CC}=20V$. Also find the value of V_{CE} and collector potential V_C .
3. The following readings were obtained experimentally for a JFET:
 $V_{GS}=0V$ and when $V_{DS}=7V$, $I_D=10mA$; when $V_{GS}=0V$ and $V_{DS}=15V$, $I_D=10.25mA$ and when $V_{GS}=0.2V$ & $V_{DS}=15V$, $I_D=9.65mA$. Determine : i) ac drain resistance
ii) transconductance and iii) amplification factor.
4. The intrinsic stand-off ratio η for a UJT=0.6. If the inter-base resistance is $10k\Omega$, what are the values of R_{B1} and R_{B2} ?
5. SIMPLIFY the logic function using K-Map and realize the logic circuit using NAND gates. $F(ABCD) = \Sigma m (1,3,7,11,15)$ and don't care $d(0,2,5)$.
6. Implement (i) EX-OR function using NOR gates. (ii) NOT function using EX-OR gate.
7. Using OpAmp IC 741, draw the Analog circuit for the following:
i) An Inverting Amplifier having a gain of -20 with an input impedance of $10K\Omega$. ii) a Non-Inverting Amplifier with a gain of $+20$.

SECTION – C

ANSWER ANY THREE QUESTIONS: (3 x 15 = 45)

8. Explain with diagram the functioning at a R-C coupled transistor amplifier with special reference to its frequency response behaviour.

9. Account for the formation of wedge shaped depletion regions and the channel construction of a JFET.
Explain the mechanism of current flow in a enhancement mode MOSFET.
10. Implement a 4-Bit Parallel Binary Adder/Subtractor circuit using Full Adders & Ex-OR gates. Explain the functioning of the Circuit with a suitable example.
11. Draw the logic circuit and explain the functioning of the following counters.
i) MOD 5 – Ripple Counter ii) Left – Shift Register.
12. Using OpAmp draw the circuit and explain the working of the following:
i) Adder ii) subtractor iii) Inverter iv) Integrator
v) Differentiator

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