STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2004-05 & thereafter)

SUBJECT CODE : PH/MC/MI54

B.Sc. DEGREE EXAMINATION NOVEMBER 2007
BRANCH III - PHYSICS
FIFTH SEMESTER

REG. No._____

COURSE : MAJOR – CORE
PAPER : MICROPROCESSORS
TIME : 30 MINS. **MAX. MARKS : 30**

SECTION - A
TO BE ANSWERED IN THE QUESTION PAPER ITSELF
ANSWER ALL QUESTIONS: **(30 x 1 = 30)**

I CHOOSE THE CORRECT ANSWER:

1. No. of ADDRESS LINES in 8085 is
   a) 8 b) 10 c) 16 d) 20

2. No. of HARDWARE INTERRUPTS in 8085 is
   a) 2 b) 4 c) 6 d) 8

3. No. of SOFTWARE INTERRUPTS in 8085 is
   a) 2 b) 4 c) 6 d) 8

4. No. of Bits the Internal DATA BUS handles at a time in 8085 is
   a) 4 b) 8 c) 10 d) 16

5. No. of MNEMONICS used in the Instruction SET of 8085 is
   a) 16 b) 40 c) 80 d) 256

6. Maximum no. of INPUT PORTS supported by direct I/O scheme in 8085 is
   a) 256 b) 512 c) 1024 d) 3

7. Minimum no. of ADDRESS LINES required for Decoding 8K× 8 ROM under Partial decoding is
   a) 10 b) 12 c) 13 d) 16

8. No. of 8 Bit I/O ports supported by one 8255 PPI chip is
   a) 2 b) 3 c) 4 d) 8

9. No. of Non-Maskable interrupts available in 8085 is
   a) 1 b) 2 c) 3 d) 4

10. No. of BITS transferred by a PUSH Instruction is
    a) 2 b) 4 c) 8 d) 16

11. The Instruction DCXB on reducing the content of BC reg-pair to 0000 H, affects which of the FLAGS in 8085?
    a) ZERO b) CARRY c) AUX CARRY d) NONE of the flags

..2

12. The Instruction MVI A, 00 H affects which of the FLAGs in 8085?
    a) ZERO b) CARRY c) AUX CARRY d) NONE of the flags

13. The contents of register B = 09 H; C = FF H; after executing the instruction INRC, the content of B register will be
    a) 00 b) 10 c) 09 d) 0A

14. The contents of register B = 09 H; C = FF H; after executing the instruction INXB, the content of C register will be
    a) 00 b) 10 c) 09 d) 0A

15. The Vector Location of the Hardware Interrupt TRAP is
    a) 0000 H b) 8000 H c) FFFF H d) 0024 H

II FILL IN THE BLANKS:

16. The instruction that enables the Serial Out Data transfer through SOD terminal in 8085 is _____.
17. The Addressing Mode which uses memory pointer for Data Transfer is _____.
18. The Instruction that does not have Execute Cycle is _____.
19. STACK in 8085 has an array of memory locations assigned to it and the array is called as _____ array.
20. The 16 BIT Accumulator available in 8085 is _____.

III STATE TRUE OR FALSE:

21. During MEMORY READ operation $IO/\overline{M}$ Line will be HIGH while $\overline{RD}$ Line will be LOW.
22. The Higher order ADDRESS BUS is Unidirectional.
23. None of the Data Transfer Instructions will affect any of the FLAGs status.
24. RST4.5 is one of the Maskable interrupts in 8085.
25. Both the INPUT PORT and the OUTPUT PORT can have the same ADDRESS.

IV ANSWER BRIEFLY:

26. What is Tri-state Buffer?

27. Name the RESTART instructions available in 8085.

28. How the IC8255 can be SET in BSR mode of operation?

29. Name the Destination Register in the DAD D instruction.

30. List the Addressing modes available in 8085 to effect DATA Transfer between MEMORY and ACCUMULATOR.

STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2004-05 & thereafter)

SUBJECT CODE : PH/MC/MI54

B.Sc. DEGREE EXAMINATION NOVEMBER 2007
BRANCH III - PHYSICS
FIFTH SEMESTER

COURSE : MAJOR – CORE
PAPER : MICROPROCESSORS
TIME : 2 ½ HOURS **MAX. MARKS : 70**

SECTION – B

ANSWER ANY FIVE QUESTIONS: **(5 x 5 = 25)**

1. Explain the Addressing Modes supported by 8085 with an example for each.
2. Write Assembly Language Instructions to perform the following:
   a) To multiply the content of C register by 7_{10} without using ADD instruction.
   b) To exchange the contents of BC reg-pair with HL.
3. Explain the statement – 'The STACK grows Downwards'.
4. Write a suitable time delay subroutine program and call it to generate a 500Hz square wave. Frequency of the crystal used is 2MHz? Account for the delay.
5. Define Exhaustive decoding. Draw the decoder arrangement for interfacing a 4K×8 ROM with 8085. If the starting address of the ROM is 0000 H, what is its END address?
6. Write program to convert a 2 digit BCD number stored in memory at location DATA to its HEX equivalent number and store the result in memory at location HEX.
7. List the difference between direct I/O and Memory mapped I/O.

SECTION – C

ANSWER ANY THREE QUESTIONS: **(3 x 15 = 45)**

8. Discuss the salient features available in the PPI chip 8255 with its functional block Diagram. Explain the Mode 0 operation of 8255 with suitable examples.

9. Explain the interrupt circuit available in 8085 along with the masking features incorporated in the circuit. Explain how the hierarchy of interrupt can be altered.

10. Draw the hardware set up required to interface a DAC with 8085 and write the required software to produce a positive ramp.

11. Bring out the differences between the following pairs of instructions:
    a) LHLD address and LDA address
    b) LDAXD and LXID, dB
    c) ADD D and DAD D
    d) RST 5 and CALL, 5555 H

12. Write an assembly language program to arrange an array of 15 numbers stored in memory in ascending order. Then move the arranged set of numbers to a new block of memory.

✂✂✂✂✂✂✂