SUBJECT CODE : PH/MC/ES54

B.Sc. DEGREE EXAMINATION NOVEMBER 2007
BRANCH III - PHYSICS
FIFTH SEMESTER

REG. No._____

COURSE	**:**	**MAJOR – CORE**
PAPER	**:**	**ELECTRONICS**
TIME	**:**	**30 MINS**

MAX. MARKS : 30

SECTION - A

TO BE ANSWERED ON THE QUESTION PAPER ITSELF

ANSWER ALL QUESTIONS: (30 x 1 = 30)

I. **Choose the correct answer:**

1. The d.c. load line of a transistor circuit
   a) is a graph between I_C and V_{CE} b) is a graph between I_C and I_B
   c) does not contain the locating point   d) is a curved line

2. The positive part of the output signal in a transistor circuit starts clipping, if Q-point of the circuit moves
   a) towards the saturation point   b) towards the cut-off point
   c) towards the center of the load line   d) none of these

3. The voltage divider biasing circuit is used in amplifiers quite often because it
   a) limits the a.c. signal going to the base
   b) makes the operating point almost independent of β
   c) reduces the d.c. base current
   d) reduces the cost of the circuit

4. When a BJT is employed as an amplifier, it operates
   a) in cut-off   b) in saturation
   c) well into saturation   d) over the active region

5. The main use of an emitter follower is as
   a) power amplifier   b) impedance matching device
   c) low input impedance circuit   d) follower of base signal

6. The voltage gain of a common base amplifier is
   a) zero   b) less than unity   c) unity   d) greater than unity

7. Two stages of multistage amplifier have gain of 50 and 20. The dB voltage gain is
   a) 3   b) 30   c) 300   d) 1000

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8. The R.C. coupling is popular in audio amplifiers because
   a) it provides an output signal in phase with the input signal
   b) it needs low voltage collector supply
   c) it has better audio frequency response
   d) none of these

9. The voltage gain of non-inverting operational amplifier is
   a) greater than unity   b) less than unity
   c) greater or less than unity   d) variable

10. An Op-amp can be classified as _____ amplifier
    a) linear   b) low r_{in} c) positive feed back   d) RC coupled

11. For an ideal difference amplifier CMRR should be
    a) as high as possible   b) as low as possible   c) constant   d) unity

12. The input stage of an Op-amp is usually a
    a) differential amplifier   b) class B push pull amplifier
    c) CE amplifier   d) level shifter

13. The unity gain frequency of an Op-amp equals
    a) 10^3 Hz   b) 10^6 Hz   c) 10^2 Hz   d) 10 Hz

14. An Op-amp has a common mode gain of 0.01 and a differential mode gain of 105. Its CMRR would be
    a) 10^{-7} b) 10^{-3} c) 10^3 d) 10^7

15. When in a negative scalar circuit both R_i and R_f are reduced to zero, the circuit functions as
    a) integrator   b) subtractor   c) comparator   d) voltage follower

II. State whether true or false:

16. The stability factor of CB circuits is '1' and therefore it requires bias stabilization.

17. DC load lines for a transistor can be drawn if the supply voltage and collector resistor are known.

18. A NOR gate with inverted inputs is equivalent to an AND gate.

19. Since input resistance of an ideal Op-amp is infinite, it becomes a current controlled device.

20. The integrator is a circuit whose output is proportional to the area of its input waveform.

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III. Fill in the blanks:

21. A NAND gate must have both inputs '1' to have its output at state

_____.

22. When simplified $A\overline{B} + \overline{AB}$ = _____.

23. According to laws of Boolean Algebra $A + AB$ = _____ and

$A + \overline{A}B$ = _____.

24. Intrinsic standoff ratio is given by _____

25. Operating point of a transistor is defined as _____.

IV. Answer the following in one or two sentences:

26. Obtain the 'sum bit' and 'carry bit' of a half adder using NAND gates only.

27. How can you realize a D latch from a JK flip flop ?

28. How many flip flops are required to realize a moduls 16 ripple counter?

29. Draw the block diagram of a 4 bit serial shift left register using flip flops.

30. Define pinch off voltage in a FET.

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TIME   :   **2 ½ hrs**   **MAX. MARKS : 70**
                         SECTION – B

ANSWER ANY FIVE QUESTIONS: **(5 x5 = 25)**

1.   Given $V_{CC} = 20V$, $R_C = 1K\Omega$, $R_E = 5K\Omega$, $R_1 = 10K\Omega$, $R_2 = 10K\Omega$, $\beta = 462$
      and $V_{BE} = 0.7V$. Calculate the emitter current and collector to emitter voltage.

2.   An amplifier has a bandwidth of 500 KHz. If the lower cut-off frequency is 25
      Hz, what is the upper cut-off frequency? Also find the voltage gain at the lower
      cut-off frequency if the mid frequency gain is 120.

3.   Figure shows the circuit of a summing amplifier.
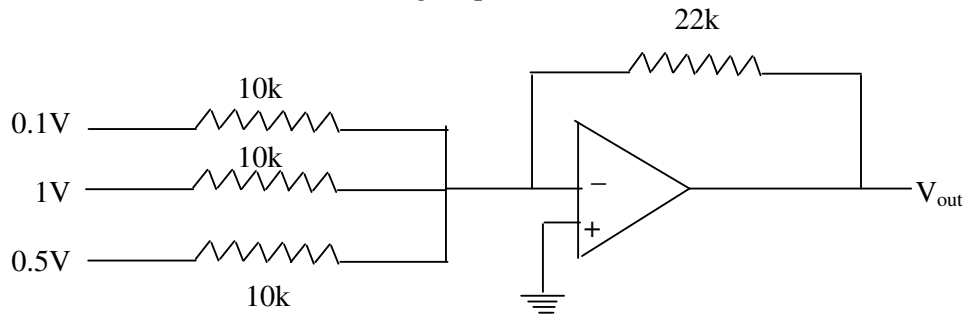
      Determine the value of output voltage for this circuit.

4.   Simplify:
      a) $Y = ABC + A\overline{B}\overline{C} + AB\overline{C}$
      b) $Y = AB + \overline{A}C + BC$

5.   Prove that NAND gates are Universal.

6.   Simplify using K-map
          $F(A,B,C,D) = \Sigma m(2,3,12,13,14,15) + \Sigma d(4,5)$
      and realize the same using 2 input NAND gates

7.   Simplify using K-map
          $F(A,B,C,D) = \Sigma m(5,9,15) + \Sigma d(2,6,7,11,12,13,14)$
       and realize the same using 2 input NOR gates

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SECTION – C

ANSWER ANY THREE QUESTIONS: **(3 x15 = 45)**

8. Give the circuit of a single stage RC coupled amplifier explain its frequency response. Also give the advantages and disadvantages of the circuit.

                                                                                (10+5)

9. Compare the construction and working of a N-channel DEMOSFET and E-MOSFET with the help of their I-V characteristics.

                                                                                (15)

10. Give the circuit and explain the working of the following in detail:
    a) Parallel Binary Adder   (5)
    b) BCD adder   (10)

11. a) Give the function table of a JK flip flop.
    b) Give the circuit, the truth table and explain the working of a MOD 6 Asynchronous Up counter.
    c) Convert the circuit into a MOD 6 down counter.   (3+8+4)

12. a) Draw the circuit of a Summing amplifier using Op-amp and write the equation for the output of the circuit.   (5)
    b) Solve the given simultaneous equations using Op-amps.   (10)

    $$2x + y = 5$$
    $$x + 4y = 6$$

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