STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2011-12)

SUBJECT CODE : 11PH/MC/SE64

B.Sc. DEGREE EXAMINATION APRIL 2014
BRANCH III - PHYSICS
SIXTH SEMESTER

REG. No._____

COURSE : MAJOR – CORE
PAPER : SEMICONDUCTOR ELECTRONICS
TIME : 30 MINS. MAX. MARKS : 30

SECTION – A
TO BE ANSWERED IN THE QUESTION PAPER ITSELF

ANSWER ALL QUESTIONS: (30 x 1 = 30)

I Choose the Correct Answer:

1. A JFET is
   (a) a unipolar device (b) a voltage controlled
   (c) a current controlled device (d) both a &b

2. In voltage divider biased npn transistor, if the upper voltage divider resistor(the one connected to vcc) opens
   (a) the supply voltage is too high (b) the transistor goes into saturation
   (c) the transistor burns out (d) transistor goes to cut-off

3. Consider the following steps /parameters
   (i) choice of device valve or transistor (ii) Choice of load circuit (iii) DC Q –Point (iv) AC input amplitude. Given the specifications of output frequency and output voltage or power, their correct sequence while designing an amplifier will be
   (a) 1,3,2 &4 (b) 1,2,3 & 4 (c) 3,2,1& 4 (d) 3,1,4&2

4. The main function of the coupling capacitor in an RC coupled emitter amplifier is to
   (a) Increase the input impedance (b) increase the output impedance
   (c) increase the gain of the amplifier (d) DC isolation

5. The unit of voltage gain is
   (a) Volts (b) mho (c) ampere (d) none of these

6. A npn transistor circuit has $\alpha = 0.985$.If $I_C = 2$ mA then the value of I_b is
   (a) 0.06mA (b) 0.003mA (c) 0.66mA (d) 0.03mA

7. To work as a linear amplifier, a transistor must operate in
   (a) The active region (b) the saturation region
   (c) cut –off region (d) none of these

8. For cascading one should use
   (a) CE configuration (b) CB configuration
   (c) CC configuration (d) all of these

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9. The DC load line of an amplifier circuit
   (a) has appositive slope (b) has a curvature
   (c) does not contain a Q –point (d) has a negative slope

10. The resolution of a D/A converter is approximately 0.45% of its full scale range. It is
   (a) A 8 bit converter (b) A 10 bit converter
   (c) A 12 bit converter (d) A 16 bit converter

11. In an R-2R ladder D/A converter, the input resistance is
   (a)not same for all the digital inputs (b)R for each input
   (c) 2R for each input (d) 3R for each input

12. An A/D converter
   (a) consist of only D/A converter with inputs and outputs interchanged
   (b) consist of only D/A converter along with some other component
   (c) never contains D/A converter
   (d) may consist of only D/A converter along with some other components

13. The voltage Gain of a voltage follower is
   (a) unity (b) less than unity (c) greater than unity (d) variable

14. The highest possible impedance is achieved with the
   (a) inverting amplifier (b) non-inverting amplifier
   (c) Differential amplifier (d) voltage follower

15. The power supply to op-amp is
   (a) +5V (b) -5V (c) +2V (d) dual power supply

II Fill in the blanks:

16. Transistor biasing represents _____conditions.
17. The input capacitor in an amplifier is the _____ capacitor.
18. In JFET when drain voltage equals the pinch off voltage, then drain current _____ with the increase in drain voltage.
19. The voltage gain of a non – inverting Voltage Op-amp is always _____than unity.
20. The resolution of a 10 bit A/D converter which has an input voltage of -10V to +10V is _____.

III State whether true or false:

21. The stability factor of a collector feedback bias circuit is less than that of base resistor bias.
22. RC coupling is used for power amplification.
23. In an UJT the P- type emitter is heavily doped.
24. The highest possible impedance is achieved with non-inverting amplifier.
25. In an averaging amplifier the input resistance is less than the feedback resistance.

IV Answer briefly:

26. Define Load line.

27. Define Current Gain.

28. What is Intrinsic Stand- off ratio?

29. Define CMRR.

30. Define Resolution.

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PAPER : QUANTUM MECHANICS AND RELATIVITY
TIME : 2 ½ HOURS MAX. MARKS : 70

SECTION – B

ANSWER ANY FIVE QUESTIONS: (5 x 5 = 25)

1. For the transistor amplifier R_1 = 10 KΩ and R_2= 5KΩ and R_C = 1KΩ and R_L=1kΩ R_E= 2KΩ and R_L = 1K Ω (i) Draw DC load line (ii) Determine the operating point.
2. In a transistor amplifier, when the signal changes by 0.02V the base current changes by 10 μA and collector current by 1mA.If collector load R_C = 5K and R_L = 10K. Find current gain, input impedance and voltage gain.
3. Explain how UJT works as a relaxation oscillator.
4. A JFET has parameters of $V_{gs(off)}$equal to -20V and I_{dss} =12mA.Plot the transconductance curve for the device using V_{GS} values of 0V,-5V,-10V,-15V and -20V.
5. For the given Op-amp parameters find the closed loop gain, input impedance and CMRR.

   A_{CM} = 0.001,A_{OL} = 180,000,Z_{in} = 1MΩ,Z_{OUT} = 80Ω(max) slew rate = 0.5V/μs
6. Explain how op- amp can be used as Integrator.
7. An R-2R DAC network has R = 10KΩ (a) Calculate the current that flows in each parallel resistor if the reference voltage is +5V and all the switches are at logical 1. (b) Calculate the output voltage when the input digital word is 1010.

SECTION – C

ANSWER ANY THREE QUESTIONS: (3 X 15 = 45)

8. What is transistor biasing? Explain base resistor method and voltage divider method in detail.
9. With a neat diagram, explain single stage RC coupled amplifier in detail and also draw the frequency response curve of the amplifier.

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10. (i) Describe the working of a JFET (5)

    (ii) Draw the V-I Characteristics of an N – channel JFET and explain the regions of importance.

    (iii) Define Drain resistance and transconductance in JFET.

11. (i) Give the characteristics of an Ideal – Op amp (ii) Draw the circuit of summing amplifier and subtract or and derive the equation for the output voltage of each circuit.

12. Describe the operation of counter type A/D converter in detail.