STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2008-09&thereafter)
SUBJECT CODE : PH/MC/MM54

B.Sc. DEGREE EXAMINATION NOVEMBER 2011
BRANCH III - PHYSICS
FIFTH SEMESTER

REG. No._____

COURSE : MAJOR – CORE
PAPER : MICROPROCESSORS AND MICROCONTROLLERS
TIME : 30 MINS. MAX. MARKS : 30

SECTION – A
TO BE ANSWERED IN THE QUESTION PAPER ITSELF

ANSWER ALL QUESTIONS: (30 x 1 = 30)

I. CHOOSE THE CORRECT ANSWER:

1. No. of CONTROL SIGNALS generated out in 8085 is,
   a) 1 b) 2 c) 3 d) 4

2. The logic status of the control signals in 8085 during Memory Read operation is,
   a) IO/M → '1' ; RD → '1' b) IO/M → '1' ; RD → '0'
   c) IO/M → '0' ; RD → '0' d) IO/M → '0' ;RD→ '1'

3. No. of Addressing modes' that support Memory to CPU Data Transfer, in 8085 is,
   a) 2 b) 4 c) 6 d) 8

4. No. of Bits the Internal DATA BUS handles at a time in 8085 is,
   a) 4 b) 8 c) 10 d) 16

5. The addressing mode best suited to transfer the content of Accumulator to a given address of a Memory location in 8085 is,
   a) Immediate b) Register addressing c) Direct addressing d) Register-Indirect

6. The 16 bit Accumulator in 8085 is,
   a) A reg b) BC rp c) DE rp d) HL rp

7. Minimum no.of ADDRESS LINES required for Decoding 8K x 8 ROM under Partial decoding is,
   a) 10 b) 12 c) 13 d) 16

8. If Pin No.A_{15} of 8085 is used to enable the chip enable pin of 8255 PPI chip the Address of PORT A is,
   a) 15 H b) 40 H c) 80 H d) A3 H

9. The Maskable Interrupt available in 8085 is,
   a) RST 4.5 b) RST 5.5 c) RST 6.5 d) RST 7.5

10. In 8085 the no. of BITS transferred by the Instruction LHLD, address is,
    a) 2 b) 4 c) 8 d) 16

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11. Which of the following Instruction CLEARs the content of Accumulator (A reg) without affecting any of the flags?
    a) MVI A, 00 H b) XRAA c) ANI, 00 H d) SUB A

12. Which of the following instruction inputs DATA through SID i/p pin of 8085?
    a) IN b) OUT c) SIM d) RIM

13. The contents of register D=09 H; E=FF H; after executing the instruction INRE, the content of D register will be,
    a) 00 b) 10 c) 09 d) 0A

14. The contents of register D=09 H; E=FF H; after executing the instruction INXD, the content of E register will be,
    a) 00 b) 10 c) 09 d) 0A

15. No. of BYTES allotted for SFR in microcontroller 8051, in its RAM Area is,
    a) 32 b) 80 c) 128 d) 256

II. FILL IN THE BLANKS:

16. If Accumulator in 8085 contains 7F H, its content after executing the instruction CMA will be ----------

17. The Addressing Mode which uses memory pointer for Data Transfer is ---------- .

18. The VECTOR ADDRESS of the hardware interrupt RST 7.5 H is ---------- .

19. The RAM area allotted for STACK in 8051 is called as ---------- array.

20. The BIT ADDRESSABLE AREA in RAM Starts from ---------- in 8051.

III. STATE WHETHER TRUE OR FALSE:

21. The destination for DAD D instruction is DE reg. pair.

22. The Higher order ADDRESS BUS is Unidirectional.

23. Partial Decoding leads to 'Memory Fold Back'.

24. RST4.5 is one of the Maskable interrupts in 8085.

25. There are 32 BYTES of working registers available in 8051 .

IV. ANSWER BRIEFLY:

26. Write Instructions to EXCHANGE the contents of BC rp with DE rp.

27. Write instructions to transmit DATA ‘1’ through SOD pin of 8085.

28. How the IC 8255 can be SET in BSR mode of operation ?

29. Write a suitable instruction to mask off RST 7.5 and allow RST 6.5 & RST 5.5 interrupts.

30. Name the MATH FLAGS available in 8051 ?.

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SECTION – B

ANSWER ANY FIVE QUESTIONS: (5 X 5 = 25)

1. Explain the Addressing Modes supported by 8085 with an example for each.
2. Explain PUSH,POP operations of the STACK & the role of Stack Pointer in 8085.
3. Bring out the differences between the following pairs of instructions:
   a. LDA, 8050 H and LXIH, 8050 H
   b. LDAXD and LHLD, 8500 H
4. Write a Program to ADD the contents of THREE consecutive Memory locations starting with 9050 H along with the content of B register and store the result SUM at 9053 H
5. What are RESTART instructions ? Explain how they function and mention the advantages in using them.
6. Write a program to determine Square root of a Single Byte number stored in memory at location DATA, and store the result in memory at location HEX.
7. What are special function registers ? Explain its role in 8051.

SECTION – C

ANSWER ANY THREE QUESTIONS: (3 X 15 = 45)

8. Discuss the salient features available in the PPI chip 8255 with its functional block Diagram. Write a program segment to BLINK (to go ON/OFF alternatively) the LEDs connected to the MSB & LSB of PORT A of the 8255 chip enabled by pin A_{14} of 8085.

9. Design a Memory Interface to provide 4K ROM and 4K RWM . Use 2Kx8 memory devices and a suitable decoder. Prepare the Address Map. What is the starting address of the RWM assuming that the RWMs are placed immediately following the EPROMs ?

10. Draw the decoder arrangement using NAND for an Input PORT with Address F5 H & an Output Port with Address F7 H in Direct I/O. Explain the decoder set-up.

11. Explain the Architecture of i) Microprocessor 8085 .and ii) Microcontroller 8051 with suitable Functional Block diagrams.

12. Explain the Hardware Interrupts available in 8085. Explain their salient features. Describe the SIM and RIM instruction formats.

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