STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2008-09)

SUBJECT CODE : PH/MC/EL64

B.Sc. DEGREE EXAMINATION APRIL 2011
BRANCH III - PHYSICS
SIXTH SEMESTER

REG. No._____

COURSE : MAJOR – CORE
PAPER : ELECTRONICS-II
TIME : 30 MINS. MAX. MARKS : 30

SECTION – A

TO BE ANSWERED IN THE QUESTION PAPER ITSELF:

ANSWER ALL QUESTIONS: (30 x 1 = 30)

I CHOOSE THE CORRECT ANSWER:

1. The stability of the circuit is poor in
   (a) collector base circuit (b) fixed bias circuit
   (c) Emitter base circuit (d) none of the above

2. In the following biasing circuit, which one has more advantages
   (a) fixed bias (b) collector to base bias circuit
   (c) emitter bias circuit (d) none of the above

3. The dc load line of a transistor circuit
   (a) has a negative slope (b) does not contain the Q – point
   (c) is a curved line (d) gives graphic relation between I_C and I_B

4. Which of the following statement is not correct
   (a) Amplifier allows a small input signal to control a large amount of power in the output
   (b) Amplifier increase the amplitude of a desired ac signal voltage
   (c) Amplifier increase the amplitude of a desired ac signal current
   (d) Amplifier generates oscillation

5. In RC coupled amplifier, the increased capacitance of the collector base junction is known as
   (a) zener effect (b) avalanche effect (c) Miller effect (d) tunnel effect

6. In RC coupled amplifier,
   (a) The voltage gain is stable in mid frequency range
   (b) The voltage gain is stable in lower frequency range
   (c) The voltage gain is stable in upper frequency range.
   (d) The current gain is constant always.

7. FET operates on
   (a) minority carriers only (b) majority carriers only
   (c) both majority and minority carriers (d) none of the these.

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8. The drain current remains constant
   (a) below the pinch – off voltage (b) above the pinch – voltage
   (c) At lower level drain voltage (d) none of these.

9. The device which has negative resistance region is
   (a) FET (b) SCR (c) TRANSISTOR (d) UJT

10. OP AMP is a
   (a) positive feedback amplifier (b) direct coupled negative feedback amplifier.
   (c) push – pull amplifier. (d) power amplifier.

11. OP AMP has
   (a) infinite input impedance (b) zero gain
   (c) zero band width (d) infinite output impedance.

12. The feed back path of an op amp integrator has
   (a) a resistor (b) a capacitor (c) an inductor (d) a transistor.

13. For a two bit DAC, the output voltage for binary 10 with 10v range is
   (a) 5v (b) 10v (c) 0v (d) 1v

14. In R – 2R ladder type DAC
   (a) wide range of resistors required (b) only single value of resistors required
   (c) only two values of resistor required (d) only three values of resistor required

15. ADC is considered as a
   (a) decoding device (b) encoding divider
   (c) waveform generator (d) voltage multiplier

II. FILL IN THE BLANKS:

16. In order to provide distortionless amplification the _____of a transistor must be biased properly.
17. In RC coupled amplifier the coupling capacitor transmit the _____ but block the _____ .
18. UJT has frequently used as _____oscillator.
19. _____ is classified as a linear amplifier.
20. _____ amplifier is used with a binary weighted network in a DAC.

III. STATE WHETHER TRUE OR FALSE:

21. dc load line is a straight line joining the cut – off and saturation point.
22. In RC coupled amplifier the voltage gain of the amplifier does not depend on the frequency range over which it operates.
23. The simulation of the UJT is a variable voltage divider.
24. op amp. can be used for amplifying both ac and dc inputs.
25. In DAC Opamp is simply working as differentiator.

IV. ANSWER THE FOLLOWING:

26. What is stability factor ?

27. What is an amplifier ?

28. Define ‘Drain resistance’

29. Define CMRR.

30. What is the difference between ADC and DAC ?

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SECTION – B

ANSWER ANY FIVE QUESTIONS: **(5 x 5 = 25)**

1. Explain dc and ac load line with suitable diagram.
2. Draw the single stage transistor amplifier circuit and explain its function.
3. Give any five difference between FET and bipolar transistor.
4. Determine the drain resistance of the FET for
   (i) V_{GS} = 0v, at V_{DS} = 5v and I_D = 0.2 mA.
   (ii) V_{GS} = -2v and V_{DS} = 8v and I_D = 0.1 mA.
5. For an UJT, η = 0.8 , VP = 10. 3 v and R_{B2} = 5 kilo ohm. Determine R_{B1} and V_{BB}.
6. Calculate the output voltage of an op amp, summing amplifier for V_1 = 1v, V_2 = 2v, V_3 = 3v, R_1 = 500 kilo ohm, $R_2 = R_3 = R_f$ = 1000 kilo ohm.
7. For a 4 bit DAC, what is the output voltage, if the input binary word is 0111 (output range is 0 to 20 v.)

SECTION – C

ANSWER ANY THREE QUESTIONS: **(3 x 15 = 45)**

8. With necessary circuit diagram, explain the voltage divider bias method. Arrive its stability factor.
9. Draw the circuit diagram of RC coupled amplifier and explain its function.. Derive the equation for its voltage gain at mid – frequency region only.
10. What is FET ? Explain the construction, working and output characteristics of a FET.
11. Draw the OP AMP inverting configuration and derive an expression for its gain. Explain, how OP AMP can be used as integrator and differentiator.
12. Explain the function of
    (i) R – 2R ladder DAC
    (ii). Counter type ADC.