STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086
(For candidates admitted during the academic year 2009-10)

SUBJECT CODE : CS/PC/PC44

M. Sc. DEGREE EXAMINATION, APRIL 2011
INFORMATION TECHNOLOGY
FOURTH SEMESTER

COURSE : CORE
PAPER : PARALLEL COMPUTING
TIME : 3 HOURS **MAX. MARKS : 100**

Section A **10 X 2 = 20**

Answer all the questions:

1. List the four memory update options possible in PRAM model and explain in brief.
2. Draw the architecture of vector supercomputer.
3. What is flow data dependence?
4. List the factors which affect the performance of an interconnection network.
5. List the three basic actor primitives in an actor object oriented model.
6. What is asynchronous message passing?
7. List any four desirable parallel language features for synchronization or for communication purposes.
8. Explain the use of temporary storage with an example.
9. List the special requirements for facilitating efficient multiprocessing.
10. What is micro tasking?

Section B **6 X 5 = 30**

Answer any six questions:

11. Explain SIMD machine model with a neat diagram.
12. What is Bernsteins's condition? Explain in detail.
13. Write short notes on multistage networks and omega networks.
14. Explain Functional and logic Parallel Programming models in detail.
15. List the Data parallelism features and explain.
16. Write the source code for bubble sort and its translation to assembly language code assuming a three-address machine.
17. Discuss about synchronous message passing.
18. Explain any one program decomposition technique.

Section C **5 X 10 = 50**

Answer any five questions:

19. Explain shared-memory multiprocessors in detail.
20. Explain Program Partitioning and Scheduling in detail.
21. Write short notes on Program flow mechanisms and explain control flow versus data flow.
22. Explain Shared-Variable Parallel programming model in detail.
23. Write an algorithm for dependence testing based on a partitioning approach.
24. Explain in detail about local and global code optimizations.
25. Explain the principles of various synchronization mechanisms for interprocess communication.

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