STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2008-09 & thereafter)

SUBJECT CODE : PH/MC/EL64

B.Sc. DEGREE EXAMINATION APRIL 2013
BRANCH III - PHYSICS
SIXTH SEMESTER

REG. No._____

COURSE : MAJOR – CORE
PAPER : ELECTRONICS-II
TIME : 30 MINS. **MAX. MARKS : 30**

SECTION – A

TO BE ANSWERED IN THE QUESTION PAPER ITSELF:

ANSWER ALL QUESTIONS: **(30 x 1 = 30)**

I CHOOSE THE CORRECT ANSWER:

1. The base of the transistor must be biased properly to provide
   a. Damped oscillation b. Distortion less amplification.
   c. Rectification d. Filter action

2. A transistor circuit employing base bias with collector feedback has greater stability than the one without feedback because
   a. I_C decrease in magnitude b. V_{BE} is decreased
   c. of negative feedback effect d. I_C becomes independent of β

3. The dc load line of a transistor circuit
   a. has a negative slope c. is a curved line
   b. gives graphic relation between I_C and I_B d. does not contain the Q –point.

4. Common emitter amplifier is characterized by
   a. Low voltage gain b. moderate power gain
   c. Signal phase reversal d. very high output impedance

5. Because of the loading effect of next stage the gain of RC coupled amplifier is comparatively
   a. large b. small c. equal d. Very large

6. In RC coupled amplifier, the increased capacitance of the collector base junction is known as
   a. zener effect b. avalanche effect c. Miller effect d. tunnel effect

..2..

7. In a JFET. The primary control on drain current is exerted by
   a. channel resistance b. size of depletion regions
   c. voltage drop across channel d. gate reverse bias

8. In a JFET, drain current is maximum when V_{GS} is
   a. zero b. negative c. positive d. equal to V_P

9. A unijunction transistor has
   a. anode . cathode and a gate b. two base and one emitter
   c. two anodes and one gate d. anode, cathode and two gates

10 .OP AMP has
   a. zero input impedance b. zero gain
   c. infinite band width d. infinite output impedance.

11. The feed back path of an op amp differentiator has
   a. a resistor b. a capacitor c. an inductor d. a transistor.

12. A differential amplifier
   a. amplifies the non inverting input signal b. amplifies the inverting input signal
   c. compare the inputs d. amplifies the difference between input signals

13. For a two bit DAC, the output voltage for binary 10 with 10v range is
   a. 5v b. 10v c. 0v d. 1v

14. In a weighted resistor type DAC
   a. wide range of resistors required
   b. only single value of resistors required
   c. only two values of resistor required.
   d. only three values of resistor required.

15. ADC is considered as a
   a. decoding device b. voltage multiplier
   c. waveform generator d. encoding device

FILL IN THE BLANKS.

16. The stability of the circuit is poor in _____ bias circuit
17. In RC coupled amplifier the coupling capacitor transmit the _____ but block the _____ .
18. UJT has _____ resistance
19. The input impedance of an ideal operational amplifier is _____
20. _____ amplifier is used with a binary weighted network in a DAC.

..3..

TRUE OR FALSE.

21. ac load line is steeper than dc load.

22. The entire frequency range of the RC coupled amplifier can be well divided into two range.

23. A JFET can be cut off with the help of V_{DD}.

24. Op Amp. can be used for amplifying ac only.

25. In DAC Op Amp is simply working as integrator.

ANSWER BRIEFLY

26. What is stability factor?

27. What is an amplifier?

28. Define 'Intrinsic standoff ratio'.

29. Define CMRR.

30. What is the difference between ADC and DAC ?

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SECTION – B

ANSWER ANY FIVE QUESTIONS: **(5 X 5 = 25)**

1. With necessary diagrams ,explain the function of an UJT.
2. Draw the single stage transistor amplifier circuit and explain its function.
3. Explain the function of OP AMP integrator and differentiator with necessary circuit diagram.
4. Determine the values of g_m at the bias(Q) point -0.5v for $\Delta I_D = 2.1mA$, $\Delta V_{GS} = 0.6v$ and at the bias(Q) point -1.5v for $\Delta I_D = 1.8mA$, $\Delta V_{GS} = 0.7v$ respectively.
5. The intrinsic standoff ratio for a UJT is 0.6. If the inter base resistance is 10 kilo ohm, determine the value of R_{B1} and R_{B2}.
6. Calculate the output voltage of an op amp, summing amplifier for $V_1 = 1v$, $V_2 = 2v$, $V_3 = 3v$, $R_1 = R_2 =$ 500 kilo ohm, $R_3 = R_f = 1000$ kilo ohm.
7. For a 4 bit DAC, what is the output voltage, if the input binary word is 0110 (output range is 0 to 10 v.)

SECTION – C

ANSWER ANY THREE QUESTIONS: **(3 X 15 = 45)**

8. With necessary circuit diagram, explain the base resistor bias method. Arrive its stability factor. Mention its advantages and disadvantages
9. Draw the circuit diagram of RC coupled amplifier and explain its function. Derive the equation for its voltage gain at mid – frequency region only.
10. What is FET ? Explain the construction, working and output characteristics of a FET.
11. Draw the OP AMP non inverting configuration and derive an expression for its gain. Explain, how OP AMP can be used as an adder
12. Explain the function of
    (i) Weighted resistor DAC
    (ii). Parallel ADC.

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