SUBJECT CODE : PH/MC/EL64

B.Sc. DEGREE EXAMINATION APRIL 2012
BRANCH III - PHYSICS
SIXTH SEMESTER

REG. No._____

COURSE   :   **MAJOR – CORE**
PAPER   :   **ELECTRONICS-II**
TIME   :   **30 MINS.**   **MAX. MARKS : 30**

**SECTION – A**

TO BE ANSWERED IN THE QUESTION PAPER ITSELF:

ANSWER ALL QUESTIONS: **(30 x 1 = 30)**

I   CHOOSE THE CORRECT ANSWER:

1. The thermal runaway of a transistor is avoided by

(a) maintaining a constant collector current   (b) maintaining a constant temperature

(c) increasing the leakage current   (d) increasing the base current

2. Which one of the following would lead to unfaithful amplification in a CE amplifier?

(a) V_{CE} falls below the Knee voltage

(b) V_{BE} goes above 0.7 V for Si transistors

(c) The base-emitter junction is properly forward biased

(d) The collector-emitter junction is properly reverse biased

3. The ratio of the slope of the DC load line to that of the AC load line is

(a) less than 1   (b) greater than 1   (c) 1   (d) 2

4. When a bipolar transistor acts as an amplifier, it is operated

(a) in its cut-off region   (b) in its saturated region

(c) well into saturation   (d) over the active region

..2..

5. RC coupled transistor amplifier has a constant gain bandwidth for

    (a) all frequencies   (b) very high frequencies

    (c) very low frequencies (d) audio frequencies

6. The phase difference between the output and input voltages of a common emitter amplifier is

    (a) 0° (b) 90° (c) 180° (d)270°

7. The channel of a JFET is between the

    (a) gate and drain   (b) drain and source

    (c) gate and source   (d) gate and either source or drain

8. The difference between the peak point and the valley point of a UJT is a measure of its

    (a) interbase resistance   (b) intrinsic stand off ratio

    (c) switching efficiency   (d) leakage current

9. After the peak point, the UJT operates in the

    (a) cut-off region   (b)saturation region

    (c) negative resistance region   (d) breakdown region

10.. The OP-AMP comparator circuit uses

    (a) positive feedback (b) negative feedback

    (c) no feedback   (d) either positive or negative feedback

11. The output V_o of the following ideal OPAMP is

    (a) 4 v   (b) 2 v   (c) 1 v   (d) -1 v

..3..
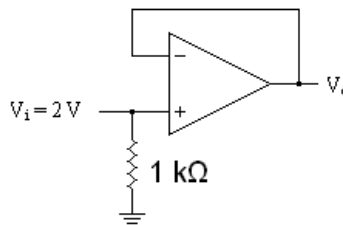
12. CMRR of 20 dB equals the numerical value

   (a) 1   (b) 2   (c) 10   (d) 20

13. In a R-2R ladder, the binary components are derived by dividing the

   (a) input voltage   (b) input current   (c) feedback voltage   (d) feedback current.

14. The reference voltage to be used in a 4 bit R-2R ladder network for a step voltage of 0.5 V is

   (a) 5 V   (b) 10 V   (c) 15 V   (d) 8 V

15. The ratio of the LSB increment to the maximum input of a DAC is its

   (a) relative accuracy (b) monotonicity (c) resolution (d) settling rate.

II   FILL IN THE BLANKS:

16. An ideal value of the stability factor is _____.

17. The fall in voltage gain from its maximum at its lower cut-off frequency of an amplifier is _____.

 18. The active component referred to double-based diode is _____.

19. A virtual ground in an OP-AMP has _____ current.

20. The number of output steps in an n-bit D/A converter is _____.

III   STATE WHETHER TRUE OR FALSE:

21. The collector current in a voltage divider biased transistor is independent of transistor parameters.

22. RC coupled amplifiers have very good impedance matching.

23. JFET has negative temperature coefficient of resistance.

24. The feedback path in an integrator circuit of an OP-Amp is a resistor.

25. The monotonicity of a DAC is a measure of its speed.

IV.   ANSWER THE FOLLOWING:

26. What is meant by Quiescent point?

27. Define bandwidth of an amplifier.

28. Draw the schematic symbol of an n-channel JFET and specify the leads.

29. Define slew rate of an OP-AMP.

30. Define Settling time of a DAC.

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SECTION – B

ANSWER ANY FIVE QUESTIONS: **(5 X 5 = 25)**

1. Arrive at an expression for the factor affecting the biasing of a transistor and explain.

2. Find the net voltage gain in db of a three stage amplifier with 100, 200, 10 as the values of voltage gain of the first, second and third stages respectively.

3. Explain the action of UJT as a relaxation oscillator with a neat sketch.

4. i) State any two characteristics of an ideal OP-AMP.

ii) Find the input current and output voltage in the following circuit.
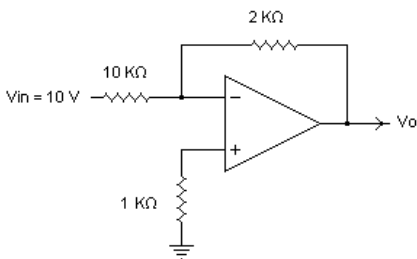
5. Calculate the Full Scale voltage and resolution of a 5 bit R-2R ladder D/A converter operated between 0 V and 10 V. Also calculate the output for the digital input 10101.

6. Draw the characteristics of a JFET and sketch the important points and parameters.

7. With a neat circuit diagram, explain the working of a differential amplifier.

SECTION – C

ANSWER ANY THREE QUESTIONS: **(3 X 15 = 45)**

8. Describe the base resistor of a transistor and arrive at its stability factor. State its advantages and disadvantages.

9. Draw the circuit of a practical single stage amplifier and explain its amplifying action.

10. With necessary diagrams, describe the construction and working of a UJT.

11. Explain the method of solving the following simultaneous equations $2x + y = 3$ and $x – y = 3$ using OP-AMPs with their experimental circuit diagram and set up.

12. i) Discuss the counter and parallel comparator methods of A/D conversion with their block diagrams.

    ii) Which method out of these two has more speed?