

B.Sc. DEGREE EXAMINATION NOVEMBER 2012
BRANCH III - PHYSICS
FIFTH SEMESTER

REG. No. _____

COURSE : MAJOR – CORE
PAPER : MICROPROCESSORS AND MICROCONTROLLERS
TIME : 30 MINS. MAX. MARKS : 30

SECTION – A

TO BE ANSWERED IN THE QUESTION PAPER ITSELF

ANSWER ALL QUESTIONS: (30 x 1 = 30)

I. CHOOSE THE CORRECT ANSWER:

1. Microprocessor 8085 can access of memory
a) 32KB b) 64MB c) 64KB d) 8MB
2. The output through the pin 37 is
a) 6.144 KHz b) 3.072 MHz c) 3.1 KHz d) 50KHz
3. The number of flags in a status register is
a) 5 b) 8 c) 16 d) 4
4. The number of maskable interrupts in 8085 is
a) 1 b) 3 c) 4 d) 6
5. Which interrupt has the highest priority?
a) INTR b) RST 6.5 c) RST 5.5 d) TRAP
6. What is the RST for the TRAP?
a) RST 5.5 b) RST 4.5 c) RST 4 d) RST 7.5
7. What is SIM?
a) Select Interrupt Mask b) Sorting Interrupt Mask
c) Set Interrupt Mask d) Serial Interrupt Mask
8. Address line for RST 3 is
a) 0020_H b) 0018_H c) 0008_H d) 0010_H
9. The addressing mode of STAX B instruction is
a) Register indirect b) Immediate c) Register direct d) Implicit
10. The instruction to clear the accumulator without affecting the flags is
a) ADD A b) SUB A c) XRA A d) MVI A, 00_H
11. If (A) = 97_H and if Cy flag =0, the content of accumulator and the status of the Cy flag after the execution of RRC instruction are
a) BC_H; Cy=0 b) CB_H; Cy=1 c) 79_H; Cy=1 d) CB_H; Cy=0
12. The instruction CMA affects which of the flags in 8085.
a) Cy flag b) S flag c) P flag d) none of the above

13. The number of input ports 8085 can interface is
a) 248 b) 258 c) 256 d) 264
14. How many 8-bit ports are there in 8255 PPI
a) 3 b) 2 c) 4 d) 1
15. The internal RAM memory of 8051 is
a) 32 bytes b) 64 bytes c) 258 bytes d) 128 bytes

II. FILL IN THE BLANKS:

16. Increment and decrement operations involving an 8-bit register do not modify flag.
17. DAA instruction is applicable only for the data in the
18. The instruction XCHG exchanges the contents of pair withpair.
19. During the execution of POP instruction the registers are saved and retrieved on basis.
20. When the address lines A_0 and A_1 of 8255 are 0 and 1 port is selected.

III. STATE WHETHER TRUE OR FALSE:

21. When the microprocessor reads the memory to take the machine code of an instruction, the memory read machine cycle is referred to as opcode fetch.
22. TRAP is a maskable interrupt.
23. Data can be transferred from one memory location to another memory location in 8085 microprocessor.
24. Microprocessor 8085 sends out the 8-bit address of the I/O ports on the higher order address lines $A_{18} - A_{15}$ only.
25. The 8051 microcontroller has two 16-bit counter/timers.

IV. ANSWER BRIEFLY:

26. Distinguish between address bus and data bus.
27. Write down the algorithm for the addition of two 8-bit numbers and to get the result in decimal form.
28. What is the function of RIM instruction?
29. What is meant by memory interfacing?
30. Mention the special registers available in 8051.

STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2008-09 & thereafter)

SUBJECT CODE : PH/MC/MM54

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SECTION – B

ANSWER ANY FIVE QUESTIONS: (5 X 5 = 25)

1. Explain the function of arithmetic and logic unit.
2. Write an assembly language program to multiply two 8-bit numbers.
3. Discuss the addressing modes of 8085 with suitable examples.
4. Explain PUSH and POP instruction with examples.
5. Write a program to move a block of 20 bytes stored at 2100_H to new memory locations starting from 2200_H.
6. Give the description of interfacing 2K X 8 ROM.
7. Discuss about interrupt controlled data transfer.

SECTION – C

ANSWER ANY THREE QUESTIONS: (3 X 15 = 45)

8. Draw the pinout diagram of 8085 and explain the function of different pins.
9. Write an assembly language program to find the smallest number of a given array of 10 numbers.
- 10.a. Discuss any four logic instructions of 8085 with examples.
b. Distinguish between I/O mapped I/O and memory mapped I/O.
11. Give the block diagram of 8255 PPI indicating different ports and show how it can be used in different modes.
12. Explain the architecture of 8051 with a block diagram.

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