STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI – 600 086.
(For candidates admitted during the academic year 2004-05 & thereafter)

SUBJECT CODE : PH/MC/MI54

B.Sc. DEGREE EXAMINATION NOVEMBER 2009
BRANCH III - PHYSICS
FIFTH SEMESTER

REG. No._____

COURSE : MAJOR – CORE
PAPER : MICROPROCESSORS
TIME : 30 MINS. **MAX. MARKS : 30**

SECTION – A

TO BE ANSWERED IN THE QUESTION PAPER ITSELF

ANSWER ALL QUESTIONS: **(30 x 1 = 30)**

I CHOOSE THE CORRECT ANSWER:

1. No. of ADDRESS LINES available is 8085 is,
   a) 8 b) 10 c) 16 d) 20

2. No. of HARDWARE INTERRUPTS in 8085 is,
   a) 2 b) 4 c) 6 d) 8

3. No. of SOFTWARE INTERRUPTS in 8085 is,
   a) 2 b) 4 c) 6 d) 8

4. No. of Bits the internal DATA BUS handles at a time in 8085 is,
   a) 4 b) 8 c) 10 d) 16

5. No. of MNEMONICS used in the instruction SET of 8085 is,
   a) 16 b) 40 c) 80 d) 256

6. Maximum No. of INPUT PORTS supported by direct I/O scheme in 8085 is,
   a) 256 b) 512 c) 1024 d) 3

7. Minimum no. of ADDRESS LINES required for Decoding 4K x 8 ROM under Partial decoding is,
   a) 10 b) 12 c) 13 d) 16

8. No. of 8 Bit I/O ports supported by one 8255 PPI chip is,
   a) 2 b) 3 c) 4 d) 8

9. No. of Non-Maskable Interrupts available in 8085 is,
   a) 1 b) 2 c) 3 d) 4

10. No. of BITS transferred by a PUSH instruction is,
    a) 2 b) 4 c) 8 d) 16

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11. The instruction DCXB on reducing the content of BC reg-pair to 0000 H, affects which of the FLAGs in 8085 ?
    a) ZERO b) CARRY c) AUX CARRY d) NONE of the Flags

12. The Instruction MVI, 00 H affects which of the FLAGs in 8085?
    a) ZERO b) CARRY c) AUX CARRY d) NONE of the Flags

13. The contents of register B=09H; C=FF H; after executing the instruction INRC, the content of B register will be,
    a) 00 b) 10 c) 09 d) 0A

14. The content of register B=09 H; C=FF H; after executing the instruction INXB, the content of C register will be,
    a) 00 b) 10 c) 09 d) 0A

15. The Vector Location of the Hardware interrupt TRAP is,
    a) 000 H b) 8000H c) FFFF H d) 0024 H

II FILL IN THE BLANKS:

16. The Instruction that enables the Serial Out Data transfer through SOD terminal in 8085 is _____
17. The Addressing Mode which uses memory pointer for Data Transfer is _____
18. The instruction that does not have Execute Cycle is_____
19. STACK in 8085 has an array of memory locations assigned to it and the array is called as _____ array.
20. The 16 BIT Accumulator available in 8085 is _____

III STATE TRUE OR FALSE:

21. During MEMORY READ operation IO/M line will be HIGH while RD line will be LOW
22. The Higher order ADDRESS BUS is Unidirectional
23. None of the Data Transfer Instructions will affect any of the FLAGs status.
24. RST 4.5 is one of the Maskable interrupts in 8085.
25. Both the INPUT PORT and the OUTPUT PORT can not have the same ADDRESS.

IV ANSWER THE FOLLOWING BRIEFLY:

26. What is LIFO ARRAY? – Where it is found in 8085?

27. Name the Software Interrupts available in 8085.

28. How the IC8255 can be SET in BSR mode of operation?

29. Name the Destination Register in the DAD D instruction.

30. List the Addressing modes available in 8085 to effect Data Transfer between MEMORY and ACCUMULATOR.

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COURSE : MAJOR – CORE
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TIME : 2 ½ HOURS **MAX. MARKS : 70**

SECTION – B

ANSWER ANY FIVE QUESTIONS: **(5 x 5 = 25)**

1. Explain the Address, Data and Control Bus structure available in 8085.
2. Explain PUSH, POP operations of the STACK & the role of Stack Pointer in 8085.
3. Describe the Addressing Modes supported by 80885 with suitable illustrations.
4. Write a suitable program to SEARCH for a given BYTE stored in Memory location 8050 H. If present place FF H at location 8051 H otherwise place 00 H.
5. Write a program to ADD the content of FIVE consecutive Memory locations starting with 9050 H along with the content of B register and a Decimal constant 100 and store the result SUM at 9055 H
6. Define Exhaustive decoding. Draw the decoder arrangement for interfacing a 2 Kx8 ROM with 8085. If the starting address of the ROM is 0000 H, what is its END address.
7. What are RESTART instructions? List the instructions available in 8085. Explain how they function and mention the advantage of using them.

SECTION – C

ANSWER ANY THREE QUESTIONS: **(3 x 15 = 45)**

8. Discuss the salient features available in the PPI chip 8255 with its functional block Diagram. Explain the Mode 0 operation of 8255 with suitable example.
9. Explain the interrupt circuit available in 8085 along with the masking features incorporated in the circuit. Explain how the hierarchy of interrupt can be altered.
10. Draw the hardware set up required to interface an ADC in Status Check Mode with 8085 and write the required software.

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11. Bring out the differences between the following pairs of instructions:
    a) MOV M,B and MVI B, 05H
    b) LDAXD and LHLD, 8500 H
    c) ADD D and DAD D
    d) RST 5 and CALL, 5555 H
12. List the differences between direct I/O and Memory mapped I/O.
    Draw the decoder arrangement for an Input PORT with Address F5 H & an Output Port with Address F7 H in Direct I/O. Can an input Port & an Output Port have the same address? Explain.

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