STELLA MARIS COLLEGE (AUTONOMOUS) CHENNAI - 600 086. (For candidates admitted during the academic year 2004-05 & thereafter)

SUBJECT CODE: PH/MC/ES54

B.Sc. DEGREE EXAMINATION NOVEMBER 2009 BRANCH III - PHYSICS FIFTH SEMESTER

				REG. No.							
		RSE : R :			MAX. MARKS : 30						
	SECTION – A										
	TO BE ANSWERED IN THE QUESTION PAPER ITSELF										
	ANSWER ALL QUESTIONS:				$(30 \times 1 = 30)$						
I		CHOOSE 7	THE CORRECT ANSW	VER:							
	1.	b. The base c. The base	or action ctor must be more heav must be N –type mater region must be very nar ector base junction must	ial. rrow.	se region.						
	2.	The cut – ir a.0V	voltage of a silicon sma b.0.2V	all signal transistor is c.0.5V	d.0.8V						
	3.	a. A high in b. A low in c. A low in	connected in common put resistance and a low put resistance and high put resistance and a low aput resistance and a hig	w output resistance output resistance. output resistance.	5						
	4.	Which of the a. Common c.Common		mplifiers has the higher b.Common-Co d. None of the	ollector						
	5.	a. Majority	et transistor (FET) opera carriers only. charged ions only.	ates on b. Minority ca d. None of the							
	6.]	For the opera. Low posi	ation of a depletion – ty tive b. High posi		•						
	7.	Which of that a. SCR	ne following acts like a c b. Tria								

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8.	a. A	vs of Boolean algebra b. AB.	c. B.	d. A			
9.	NOR –NOR networa. OR-AND.	rk is equivalent to b. AND –OR	c. OR –NOT	d. OR –XOR.			
10.	Mod. 16 Ripple cou	nter is constructed us b. 4	ing Flip –Flo c. 8	ops d. 16.			
11.	CMRR of an Op.Ana. Ad / Ac	mp. is b. Ac / Ad	c. Ad + Ac	d. Ad + Ac			
12	. Which of the follow a. High gain c. High input imped	ving characteristics do ance.	not necessarily appl b. low power d. Low output impo				
13.	The highest possible a. Inverting amplific c. Differential ampli		ed with the b. Non – inverting amplifier. d. Voltage follower.				
14.	The output voltage ovoltage on the input a. 0.667 V/µs		es 8V in 12μs in respo c. 1.5 V/μs	onse to a step d. 96 V/μs			
15.	15. The feedback path in an op- amp differentiater consists of a. a resistor b. A capacitor c. A resistor and capacitor in series d. A resistor and capacitor in parallel						
STATE TRUE OR FALSE:							
16	6. When the collector junction in transistors is biased in reverse direction and the						
	emitter junction in the forward direction ,the transistor is said to be in active						
	region						
17	7. A UJT acts like a diode and two resistors.						
18	3. The d.c load line of a transistor circuit is a curved line.						

19. A shift register is mainly useful for connecting parallel data to serial data and

20. A NOR gate will have an output only when all the inputs are high.

II

vice versa.

III FILL IN THE BLANKS:

	at its emitter terminal.
24.	A UJT can be switched ON from its OFF position by applying a
24.	Boolean Rule $A(A + B) = \dots$
23.	The voltage gain of a non inverting op- amp amplifier is always
22.	The voltage divider biasing circuit is used in amplifiers quite often because it
	5.6 mA . The value of α is
21.	In CB connection the emitter current is 5.8mA and the collector current is

IV ANSWER THE FOLLOWING BRIEFLY:

- 26. Define β of a transistor.
- 27. What are the conditions for proper biasing a transistor.
- 28. What is the stability factor for a common emitter circuit?
- 29. What is the open loop voltage gain of op amp.?
- 30. What is a shift register?

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COURSE : MAJOR - CORE PAPER : ELECTRONICS TIME : 2½ HOURS

TIME : 2½ HOURS MAX. MARKS : 70

SECTION - B

ANSWER ANY FIVE QUESTIONS:

 $(5 \times 5 = 25)$

- 1. Determine the d.c bias voltages and currents for a voltage divider bias circuit using PNP transistor. The circuit has V_{CC} =12 V; R_C =2 K Ω ; R_E = 1 K Ω ; R_1 = 100 K Ω and R_2 = 20 K Ω .
- 2. The data sheet of a JFET indicates that $I_{DSS} = 15 \text{mA}$ and $V_{GS \text{ (off)}} = -5 \text{ V}$. Determine the drain current for $V_{GS} = 0 \text{V}$, -1 V, -2 V and -4 V.
- 3. What is a full adder? Explain how a full adder is built using two half adders.
- 4. Show that NAND gate is a universal gate.
- 5. Show that (A+B)(B+C)(C+D) = AB + BC + CA.
- 6. Simplify using K map Y = F (A, B,C, D) = \sum (0,1,3,5,7,9,11,12,13,14,15).
- 7. For an Op –Amp ,the input voltages are $100\mu V$ and $80\mu V$. The open loop gain of the Op-Amp is 100,000. Calculate the output voltage when a) CMRR is infinity b) CMRR is 20 dB.

SECTION - C

ANSWER ANY THREE QUESTIONS:

 $(3 \times 15 = 45)$

- 8.Describe the working of a two stage R C coupled transistor amplifier .Explain the frequency response.
- 9. Explain the V-I characteristics of UJT .Discuss the working of UJT as a relaxation oscillator.
- 10. Explain K map method of solving expressions.
- 11. Discuss the working of Op.Amp. as (i) Inverting Summing Amplifier (ii) A differentiator (iii) Voltage follower.
- 12. Draw the circuit of a 4 –bit ripple counter using JK flips flops and explain its working.